Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Previously Presented) An apparatus, comprising:

a variable speed bus, the variable speed bus initialized with a first clock frequency;

a first unit coupled to the variable speed bus, the first unit having a first rate of requests to access the variable speed bus;

a second unit coupled to the variable speed bus, the second unit having a second rate of requests to access the variable speed bus; and

an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate.

2. (Original) The apparatus of claim 1, wherein the first unit is a processor unit.

3. (Original) The apparatus of claim 1, wherein the second unit is a video processor unit.

4. (Original) The apparatus of claim 1, wherein the first unit is a hard disk drive controller unit.

5. (Original) The apparatus of claim 1, wherein the second unit is an isochronous data transfer unit.

6. (Canceled).

7. (Previously Presented) The apparatus of claim 5, wherein the isochronous data transfer unit is a 1394 controller unit.

8. (Previously Presented) The apparatus of claim 5, wherein the isochronous data transfer unit is a USB controller unit.

9. (Canceled).

10. (Previously Presented) A system, comprising:

a device coupled to a variable speed bus, the device having a rate of request to access the variable speed bus; and

a clock throttling logic to adjust a clock frequency associated with the variable speed bus based on the rate of request to access the variable speed bus from the device.

11. (Previously Presented) The system of claim 10, further comprising:

an arbitration and bus control unit to monitor the rate of request to access the variable speed bus from the device and to instruct the clock throttling logic to adjust the clock frequency associated with the variable speed bus the device's rate of request to access the variable speed bus.

12. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is a processor.

13. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is a video processor.

14. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is a hard disk drive controller.

15. (Original) The system of claim 10, wherein the device coupled to the variable speed bus is an isochronous data transfer controller.

16. (Canceled).

17. (Previously Presented) The system of claim 15, wherein the isochronous data transfer controller is a 1394 controller.

18. (Previously Presented) The system of claim 15, wherein the isochronous data transfer controller is a USB controller.

19-20. (Canceled).

21. (Previously Presented) The apparatus of claim 1, further comprising:

a clock throttling unit to adjust the clock frequency of the variable speed bus to the second clock frequency according to an instruction from the arbitration and bus clock control unit.

22 (Previously Presented) The apparatus of claim 21, wherein the arbitration and bus clock control unit determines the second clock frequency based on a first bandwidth requirement from the first unit and a second bandwidth requirement from the second unit, the first bandwidth requirement derived from the first rate of request to access the variable speed bus from the first unit, the second bandwidth requirement derived from the second rate of request to access the variable speed bus from the second unit.

23. (Previously Presented) The apparatus of claim 21, wherein the variable speed bus, the first unit, the second unit, the clock throttling logic and the arbitration and clock control unit are located on a single semiconductor die.

24 (Previously Presented) The system of claim 11, wherein the arbitration and bus clock control unit determines a new clock frequency based on a bandwidth requirement from the device, the device's bandwidth requirement derived from the device's rate of request to access the variable speed bus and instructs the clock throttling logic to adjust the clock frequency of the variable speed bus to the new clock frequency.